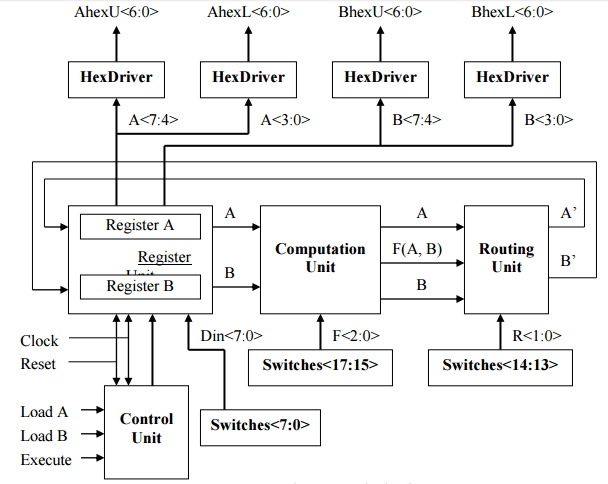
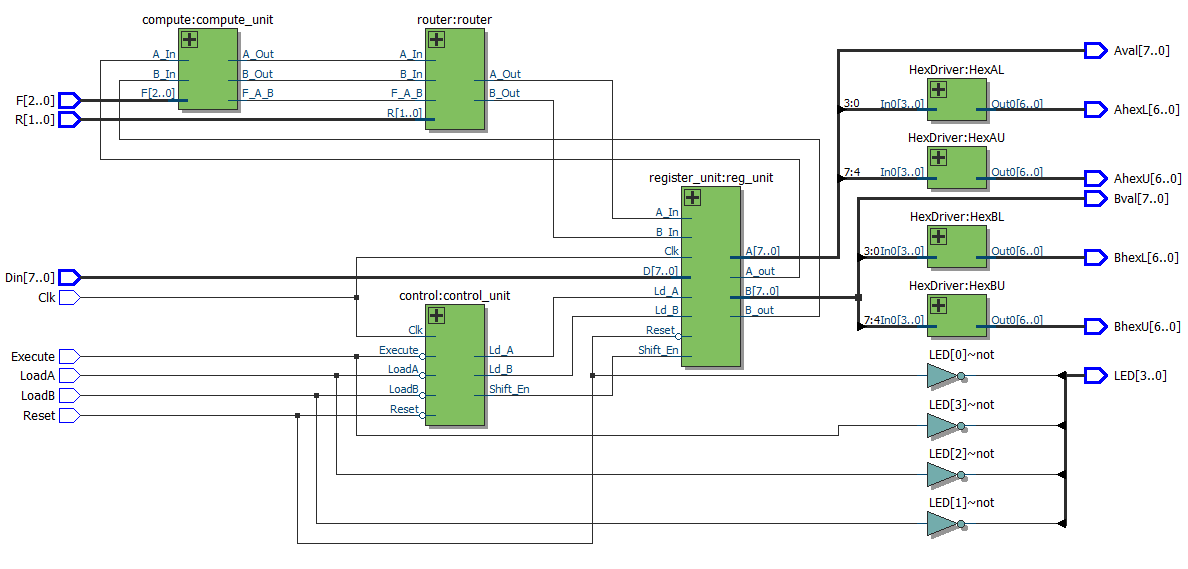
Lab 4

# Intro

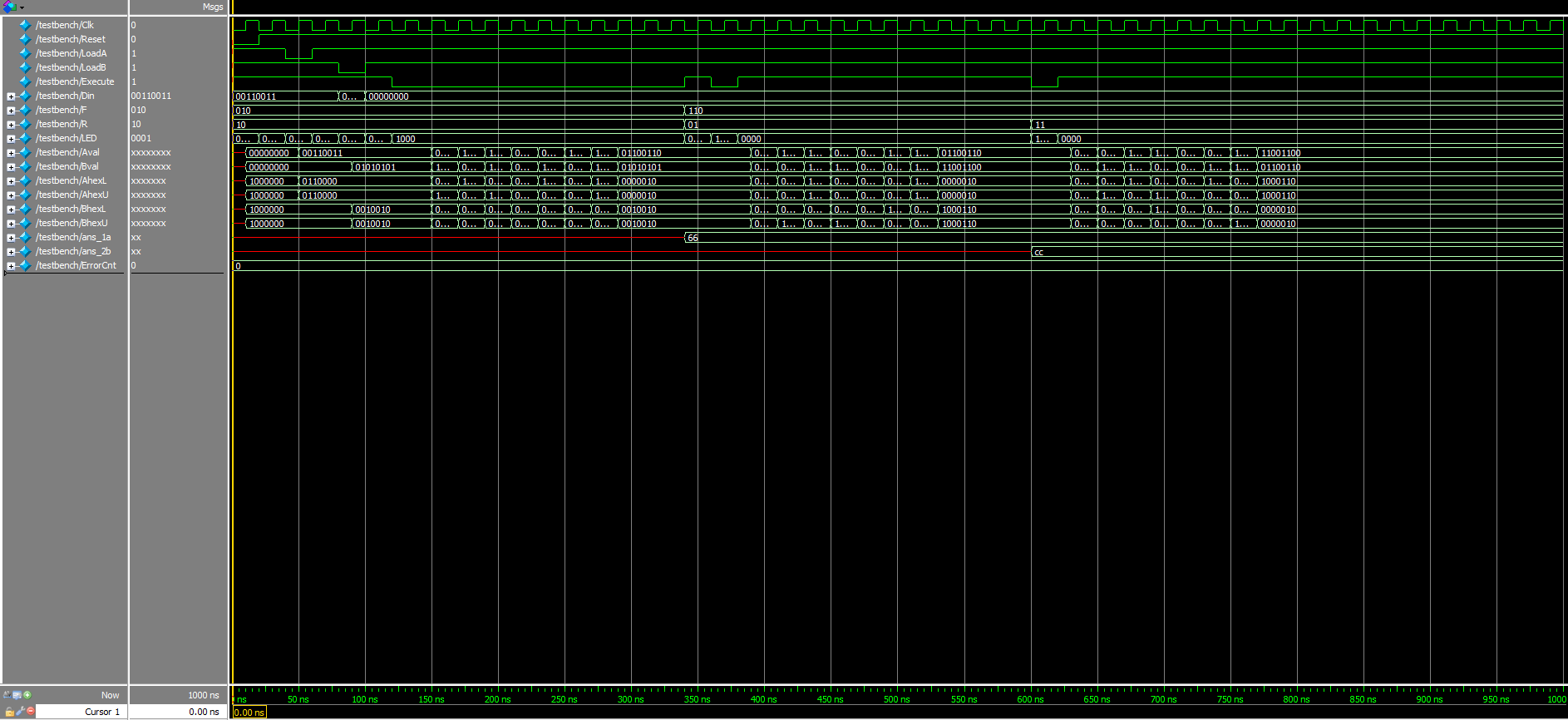
The objective of this lab was to familiarise ourselves with System Verilog and to utilise the features available to us on Altera to test features of circuits. To do this we took the example of 3 different types of adder configuration. We had the Carry Ripple Adder, The Carry Select Adder and the Carry Lookahead Adder. Firstly we had to code the different adders using Verilog and then we had to run the test tools on Altera to compare aspects of the circuit. In this lab it was mostly a trivial experiment, however, it was mainly introduced to show us the capabilities of the software going forward. We programmed our FPGA with each adder configuration and tested their functionality.

# Schematic of Bit-Serial Logic Processor





# Annotated design Simulation of Bit-Serial Logic Processor

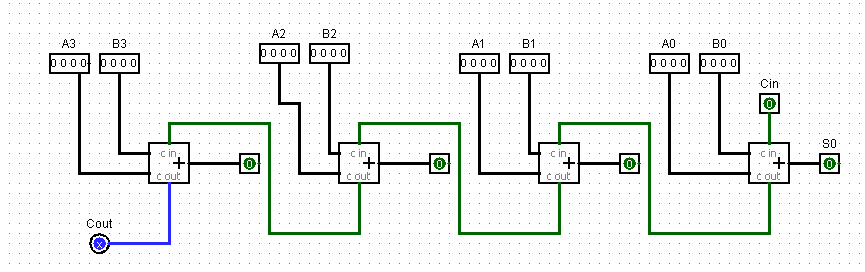


# Written Description

# Written purpose and operation

# Schematics for adder configurations

Carry Ripple Adder



Carry Select Adder

# Design Analysis Comparison from Pre-Lab

|  |  |  |  |
| --- | --- | --- | --- |
|  | Carry-Ripple | Carry-Select | Carry-Lookahead |
| Memory (BRAM) | 0 | 0 | 0 |
| Frequency | 198.53MHz | 256.81MHz | 189.14MHz |
| Total Power | 139.11MW | 139.11MW | 139.11MW |

# Post Lab Questions

1. LUT MEMORY OF PROCESSOR

|  |  |  |  |
| --- | --- | --- | --- |
|  | Carry-Ripple | Carry-Select | Carry-Lookahead |
| LUT | 114 | 123 | 114 |
| DSP | 0 | 0 | 0 |
| Memory (BRAM) | 0 | 0 | 0 |
| Flip-Flop | 3 | 4 | 2 |
| Frequency | 198.53MHz | 256.81MHz | 189.14MHz |
| Static Power | 98.5mW | 98.5mW | 98.5mW |
| Dynamic Power | 0 | 0 | 0 |
| Total Power | 139.11MW | 139.11MW | 139.11MW |

# Conclusion

Our Lab went quite smoothly this week apart from two small hiccups. Firstly we misread the tutorial and believed we had to design our own processor and synthesize it in order to get the demo point. We quickly realised that it was fine to use the processor provided to us.

Secondly, for our Carry-Select adder we had coded our MUXs wrong as we were only giving them single inputs instead of the 4 inputs they needed to select the correct Carry Out. We noticed this quite quickly after asking to demo for the lab and corrected the problem.

All in all the lab went extremely smoothly. The introduction to Verilog and the tutorial were very beneficial and we believe we have wrapped our head around the concepts of Verilog explained to us thus far. We also appreciate that Verilog is an extremely useful tool to design circuits as we found it much easier to write the code and program our FPGA than to design the entire circuit using TTL. We also appreciate the amount of physical space one can save by using an FPGA, rather than designing the entire circuit on a breadboard using transistors. It was also quite easy to debug the code as the compiler helped you locate the source of your problem, rather than in a TTL design where you would have to isolate each chip to find the issue.